REMARKS

STATUS SUMMARY

Claims 1-27 are pending in the present application. The Examiner has rejected claims 1-5, 8-15, 18-25, and 27 under 35 U.S.C § 102(e) as being anticipated by U.S. Patent No. 6,052,032 to *Järvinen* (*Järvinen*), and has also rejected claims 6, 7, 16, 17, and 26 under 35 U.S.C § 103(a) as being unpatentable over *Järvinen*.

These formal matters identified in the Office Action are addressed herein below.

RESPONSE TO CLAIM REJECTIONS UNDER 35 USC § 102(e)

The Examiner has rejected claims 1-5, 8-15, 18-25, and 27 under 35 U.S.C §102(e) as being anticipated by U.S. Patent No. 6,052,032 to *Järvinen*. MPEP § 2131 provides:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. " *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). ... "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, ...

Järvinen does not teach each and every claimed element of claims 1-5, 8-15, 18-25, and 27. Therefore, Applicants respectfully traverse these rejections.

CLAIMS 1 and 11

Claim 1 states:

> A constant current bias circuit comprising:
> an at least one resistor; and
> a bias voltage input terminal for receipt of a bias voltage connected to the at least one resistor by an electrical path resulting in a bias current when the bias voltage is present.

Claim 11 states:

> A constant current bias circuit comprising:
> an at least one resistor; and
> means for receiving a bias voltage connected to the at least one resistor by an electrical path resulting in a bias current when the bias voltage is present.

The Examiner states: "[r]egarding claims 1, 11, *Järvinen* (Figs 1-3) discloses an amplifier circuit comprising: a resistors (not label); and a bias voltage input terminal (V_{bias}) for receiving bias voltage connected to the resistor (not label) resulting [in] a bias current via the resistor, wherein the bias voltage is always present in the reference circuit and the resistor (not label) is a resistor connected between the base of transistor (Q2) and the bias voltage (V_{bias})."

In response, Applicants respectfully disagree that *Järvinen* teaches each and every aspect of the claimed invention in claim 1 either explicitly or impliedly as required under 35 U.S.C. § 102(e) and MPEP §§ 706 and 2131. First, with reference to the resistors shown in FIGs. 1-3 of *Järvinen*, the Examiner does not specify which resistor in *Järvinen* corresponds to the at least one resistor of claim 1, that is, a resistor connected to a bias voltage input terminal "by an electrical path resulting in a bias current." In other words, this element must be shown in as complete detail in *Järvinen* as it is in claim 1.

In the claimed invention, 15KΩ resistor 104 is connected to a bias voltage input terminal 102. Resistor 104 is paired with another 15KΩ resistor 106, and the output from this voltage divider resistor pair is connected to the negative input terminal of an op-amp 110. (Page 3, line 19, through page 4, line 2.) The output of the op-amp 110 is connected to the gate of a CMOS FET 114. The CMOS FET 114 has a source that is connected to the voltage supply terminal 116 and a drain connected to the positive input terminal of the op-amp 110 and a 4.7KΩ resistor 120. (Page 4, lines 3-7.) When two volts is applied to bias voltage input terminal 102, CMOS FET 114 is activated, allowing current to flow through 4.7KΩ resistor 120, which results in an I_{bias} current. (Page 5, lines 2-7.)

The claimed invention is a constant current biasing circuit. Thus the transistors are biased by choosing voltage as the dependent variable and the current in the devices is the same but the voltage varies. Thus the I_{bias} current, which has a direct relationship to the bias voltage applied to the bias voltage input terminal, is mirrored with selectable MOS FET 115 to produce the I_{ref} current that is then sourced into the collector of the bipolar junction transistor ("BJT") 126. (Page 5, lines 8-16.) The feedback loop 137 adjusts the base voltage of BJT 126 to maintain a collector current equal to I_{ref}. (Page 5, lines 17-19.)

These elements are not found in FIGs. 1-3 of *Järvinen* cited by the Examiner. FIGs. 1 and 2 show radio frequency amplifiers without and with a temperature compensation circuit, respectively. (Col. 3, lines 20-23.) FIG. 3 of *Järvinen* shows one embodiment of the invention, which is a radio frequency amplifier comprising a power

transistor, a control transistor, a control transistor, and a differential amplifier. In general, *Järvinen* discloses providing an additional control transistor arranged to conduct a current density substantially identical to that of the power transistor of the amplifier, and a feedback signal for controlling biasing of the power transistor. (Col. 2, lines 4-9.) Specifically, *Järvinen* teaches changing the collector current of the power transistor Q1 in response to a change in the collector current of the control transistor Qc. (Col. 4, lines 14-31.)

In summary, the claimed inventions of claims 1 and 11 teach a constant current bias circuit comprising an at least one resistor; and a bias voltage input terminal for receipt of a bias voltage connected to the at least one resistor by an electrical path resulting in a bias current. *Järvinen* does not set forth each and every element of claim 1, either expressly or inherently; specifically, *Järvinen* does not describe a biasing circuit that *result[s] in a bias current* when a bias voltage is present at a bias voltage terminal.

Thus, Applicants believe that independent claims 1 and 11 are in condition for allowance and respectfully request that the Examiner withdraw the rejections of these claims.

CLAIMS 2 and 12

Claims 2 and 12 are dependent on allowable claims 1 and 11, respectively, and thus are distinguishable over *Järvinen* for at least the same reasons. Therefore, Applicants believe that claims 2 and 11 are also in a condition for allowance and respectfully request that the Examiner withdraw the rejections of these claims.

Moreover, claim 2 claims a clamp circuit coupled by an electrical path to the at least one resistor that provides a minimum current. The clamp circuit 112 activates to maintain a minimum voltage at the negative input terminal of the operational amplifier 110. (Page 5, line 23, through page 6, line 1.) Diode-connected transistors Q3 and Q4 in FIG. 2 of *Järvinen* are connected between the base of the driver transistor Q2 and ground, and their purpose is to maintain the power transistor base current substantially constant by tracking the voltage drop across the base-emitter junctions of the driver transistor Q1 and the driver transistor Q2. (Col. 1, lines 40-48.)

Thus *Järvinen* also fails to disclose or describe all of Applicants' claim limitations in dependent claims 2 and 12 as well.

CLAIMS 3-5, 8-10, 13-15, and 18-20

Claims 3-5 and 8-10 are dependent on allowable claim 1, and claims 13-15 and 18-20 are dependent on allowable claim 11, and thus are distinguishable over *Järvinen* for at least the same reasons. Therefore, Applicants believe that claims 3-5, 8-10, 13-15, and 18-20 are also in a condition for allowance and respectfully request that the Examiner withdraw the rejections of these claims.

CLAIM 21

Claim 21 discloses:

> A method for constant current biasing, comprising:
> receiving an input bias voltage; and

generating a bias current by at least one resistor being in receipt of the input bias voltage.

Claim 21 is pending in the present application and has been rejected by the Examiner in the Office Action Summary page of the Office Action. The Examiner, however, has not identified claim 21 as rejected within the Office Action and has not given any references or reasons for rejecting claim 21. Therefore, Applicants believe that claim 21 is in allowable form because the Examiner has failed to show under 37 C.F.R §1.104 that any reference teaches each and every element or feature recited in the claim.

Applicant notes that 37 C.F.R §1.104(a)(2) states that:

> The applicant, or in the case of a reexamination proceeding, both the patent owner and the requester, will be notified of the examiner's action. *The reasons for any adverse action or any objection or requirement will be stated in an Office action and such information or references will be given as may be useful in aiding the applicant, or in the case of a reexamination proceeding the patent owner, to judge the propriety of continuing the prosecution.*

Additionally, 37 C.F.R §1.104(c)(2) states that:

> *In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command.* When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

The Examiner has not cited any references in rejecting claim 21; therefore, Applicants believe that claim 21 is in allowable form.

As noted above, in the Office Action, the Examiner states: "[r]egarding claims 1, 11, *Järvinen* (Figs 1-3) discloses an amplifier circuit comprising: a resistors (not label); and a bias voltage input terminal (V_{bias}) for receiving bias voltage connected to the

resistor (not label) resulting [in] a bias current via the resistor, wherein the bias voltage is always present in the reference circuit and the resistor (not label) is a resistor connected between the base of transistor (Q2) and the bias voltage (V_{bias})." Claim 21 is a method claim, and if claim 21 is rejected for the same reasons as claims 1 and 11, Applicants would respond inn the same manner as they did to the rejection of claims 1 and 11.

Therefore, *Järvinen* fails to disclose or describe all of Applicants' claim limitations in independent claim 21. Thus, Applicants believe that independent claim 21 is in condition for allowance and respectfully request that the Examiner withdraw the rejection of claim 21.

CLAIMS 22-25 and 27

Claims 22-25 and 27 are dependent on allowable claim 21. Therefore, Applicants believe that claims 22-25 and 27 are also in a condition for allowance and respectfully request that the Examiner withdraw the rejections of these claims.

RESPONSE TO CLAIM REJECTIONS UNDER 35 USC § 103(a)

The Examiner has rejected claims 6, 7, 16, 17 and 26 under 35 U.S.C § 103(a) as being unpatentable over *Järvinen*. Specifically, the Examiner acknowledges that *Järvinen* does not disclose the type of transistor used and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the transistors of the reference circuit with a Complementary Metal Oxide Semiconductor ("CMOS") or Gallium Arsenide Semiconductor. The Examiner also states that the

Applicants have not disclosed that CMOS or Gallium Arsenide Semiconductor "solves any particular problem or is for any particular purpose."

Applicants respectfully traverse these rejections. First, Applicants believe, for the reasons stated in response to the rejection of claims 1, 11 and 21 under 35 U.S.C §102(e), that even if *Järvinen* and the elements disclosed in claims 6, 7, 16, 17 and 26 were combined, the combination would not teach all of elements of these claims. In other words, *Järvinen* does not anticipate claims 1, 11 or 21, and therefore, cannot anticipate claims 6, 7, 16, 17 or 26 when combined with the appropriate additional element, i.e., a CMOS or Gallium Arsenide Semiconductor.

Moreover, Applicants believe that the Examiner has failed to establish a *prima facie* case of obviousness as required by 35 U.S.C. §103(a), the applicable case law and MPEP §2142 because the Examiner has failed to show all of the following: 1) a motivation or suggestion to combine *Järvinen* and the additional elements, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference (i.e., *Järvinen*) or to combine reference teachings; 2) a reasonable expectation of success; and 3) that *Järvinen* and the additional elements when combined teach or suggest all the claim limitations.

The MPEP § 2142 specifically states that the "examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness." Additionally, MPEP § 2142 also states that the "initial burden is on the

examiner to provide some suggestion of desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'" Official notice unsupported by documentary evidence should only be taken by the examiner when the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. MPEP § 2144.03 A.

Specifically, the Examiner has failed to show that there is a suggestion or motivation to replace the transistors of *Järvinen* with a CMOS or Gallium Arsenide Semiconductor.

Finally, as to the Examiner's statements regarding the Applicants' failure to disclose any purpose for having the at least one resistor in a first material in a substrate and at least one component of a plurality of components in a second material, this is explained on page 6, lines 3-21, of the specification. As one example, a CMOS fabrication process may be used in fabricating the bias circuit using field effect transistors ("FETs"), which are voltage driven devices that have a high input impedance, while a Gallium Arsenide ("GaAs") heterojunction bipolar transistor ("HBT") fabricating process may be used for the second circuit. The purpose is to enhance the performance of each circuit by taking advantage of the electrical characteristics of each fabrication process.

Based on the foregoing, Applicants respectfully submit that Examiner's statements regarding the combination of *Järvinen* and the other features known in the art are without foundation and cannot support a *prima facie* conclusion of obviousness.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action..

Respectfully submitted,
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Dated: July 22, 2005

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